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ORIGINAL ARTICLE

Design of Smart Card Chip Reader Based on STM32

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Abstract: This paper designs a smart card chip reader based on STM32, and gives a block diagram of the overall design of the system. It introduces the design of the peripheral hardware circuit of the main control chip STM32F103CBT6 and the RF processing chip THM3070, and the format of data communication between each part and flow chart. The communication between the host computer and the reader adopts the USB CCID protocol, which supports the USB full-speed communication rate of 12Mbps, improves the interrupt response, and overcomes the shortcomings of the traditional serial port-based readers with low communication speed and poor interrupt response. At the same time, it realizes data interaction with the PC/SC standard PC application and has better versatility.

Keywords: Circuits and Systems; Reader; STM32; USB CCID; THM3070; PC/SC

Introduction

Radio Frequency Identification (RFID) is a kind of automatic identification technology, which realizes non-contact two-way data communication through radio frequency 35 mode, identifies targets and obtains data[1]. At the same time, the identification of RFID does not need manual intervention, it can work normally in a relatively harsh environment. Radio frequency identification system is usually mainly composed of two parts: read/write module (i.e. card reader) and electronic transceiver (i.e. card). The card reader transmits a signal with a specific frequency rate through the antenna. When the card enters the radio frequency field of the antenna of the card reader, induced current will be generated, and the card will acquire energy and be activated.

The chip then sends the encoded information through the antenna built in the card, and the card reader antenna receives the carrier signal sent by the card number, then demodulate it, the demodulated and decoded information will be sent to the main controller, and finally the main controller will make corresponding processing according to different settings.

In the smart card issuing company, the traditional card writing method is to package the chip and antenna coil into a card with a plastic mold. After that, the card is initialized by means of antenna coil induction. Due to the complex electrical environment in the factory and the large radiation field of the card reader antenna during batch operation, the carrier signals emitted by different card readers interfere with each other, which may lead to the initial card.

In addition, some smart card chips are bad when they leave the factory. If these bad chips and antenna coils are packaged into cards with plastic molds before operation, the waste of coils and plastic molds will be caused and the production cost of enterprises will increase. Based on this, this paper designs a reader-writer that directly operates the smart card chip. At present, most of the card readers in the market are realized by single chip microcomputer and serial communication. The data transmission rate and interrupt response speed of this communication mode have great limitations. USB is an efficient, fast and economical serial communication interface, its ease of use and scalability has

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been widely supported and applied in the industry[2]. This design adopts USBCCID protocol as the communication mode between reader and PC, which has higher transmission efficiency and response speed than traditional serial communication, and is compatible with PC application program conforming to PC/SC standard.

1. Overall design of system

The card reader designed in this paper mainly includes: (1) the control circuit with STM32 controller as the core, and the corresponding clock 55 circuit and power supply circuit; (2) SPI communication magnetic coupling isolation circuit with adum3151 as the core; (3) The smart card chip data processing circuit with THM3070 as the core includes corresponding filtering and envelope detection circuits. As shown in Figure 1. The STM32 controller controls the whole system. It can receive commands from the upper computer and send them to after analysis.

THM3070, at the same time it will also THM3070 feedback information back to the upper computer. The main work flow of the system is as follows: the card reader is connected to the upper computer through the USB interface, and the USB module in the STM32 at this time. The block starts to enumerate the card reader as a CCID device, and then the controller will wait for the upper computer program to send instructions. When it receives the APDU command from the host computer, it will analyze it according to the format of the CCID protocol. The analyzed commands are transmitted to the radio frequency processing chip THM3070 through the SPI protocol, and then the THM3070 converts these commands into radio frequency signals and sends them to the smart card chip. The response signal returned by the smart card chip is sent to THM3070 after envelope detection. Then it is transmitted back to STM32 through SPI interface. STM32 packages the information into CCID protocol format and uploads it to the upper computer.

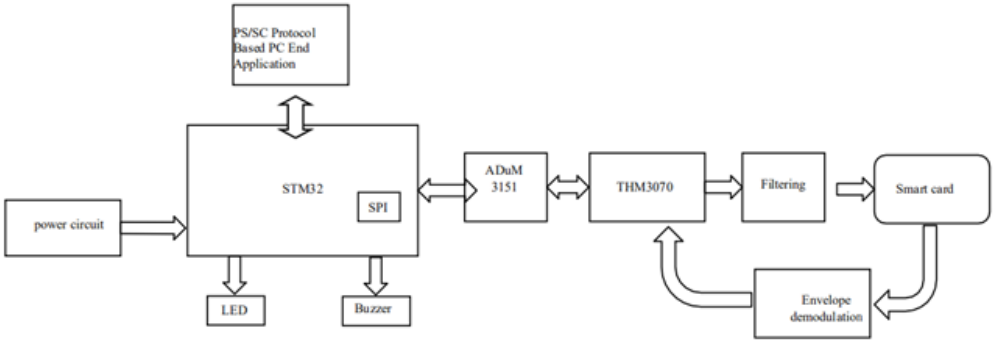

Figure 1. System overall design.

2. Hardware circuit design

2.1 Main controller and its peripheral circuits

2.1.1 Master circuit

In this design, STM32F103CBT6 is used as the main control chip to complete the scheduling of all interfaces and the processing of events. 75 STM32 is a 32 bit single chip computer designed by stmicroelectronics Company. It is based on the ARM Cortex-M3 core, which reduces the power consumption of the system and has the characteristics of high performance and low cost. The highest operating frequency of STM32F103CBT6 is 72MHz with fast interrupt response capability. The SPI interface has a full duplex and half duplex communication rate of 18 Mbit/s in slave or master mode. The 3 bit prescaler can generate 8 main mode frequencies and can be configured as 8 bits or 16 bits per frame. CRC generation/verification of hardware supports basic SD card and MMC mode, and all SPI interfaces can use DMA operation. STM32F103CBT6 is embedded with a USB device, which follows the USB full-speed standard and can realize full-speed (12Mbps) device functions; It has software configurable endpoint and standby /recovery function; The dedicated 48MHz clock is directly generated by the internal master PLL.

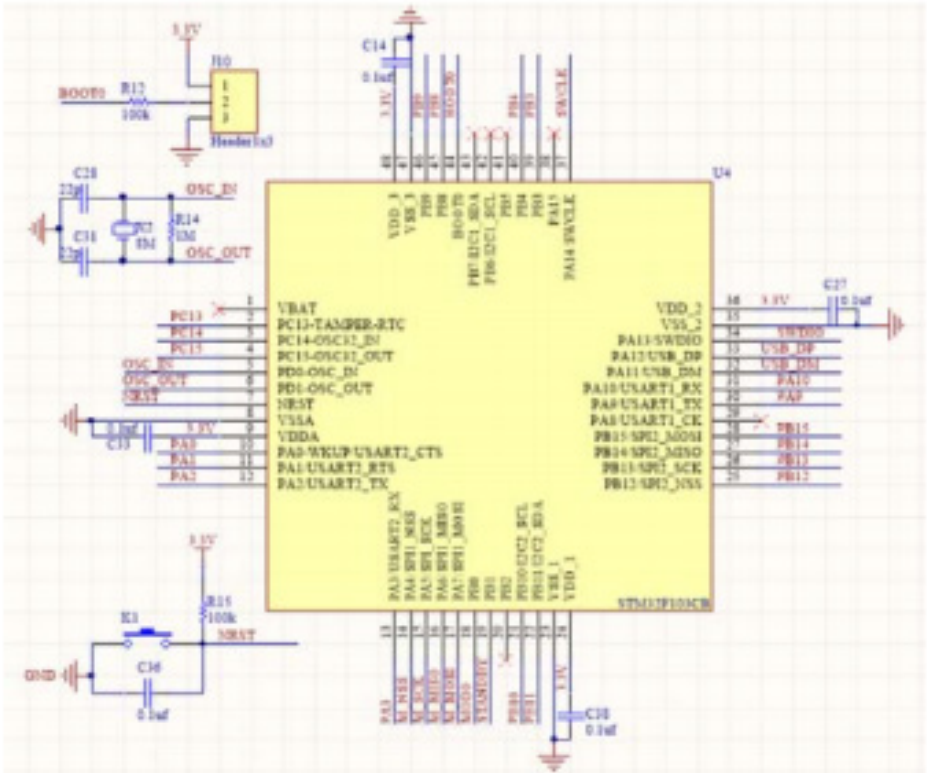

Figure 2. Main controller circuit.

2.1.2 SWD interface circuit

SWD (Serial Wire Debug) means serial debugging. Through this interface, program downloading and debugging of the chip can be realized. Compared with 20 pins of JTAG, SWD only needs 4 pins and occupies less GPIO ports.

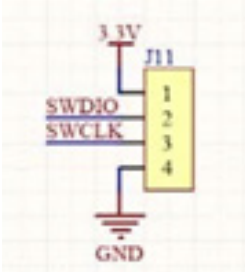

Figure 3. SWD interface circuit.

2.1.3 Buzzer and LED circuit

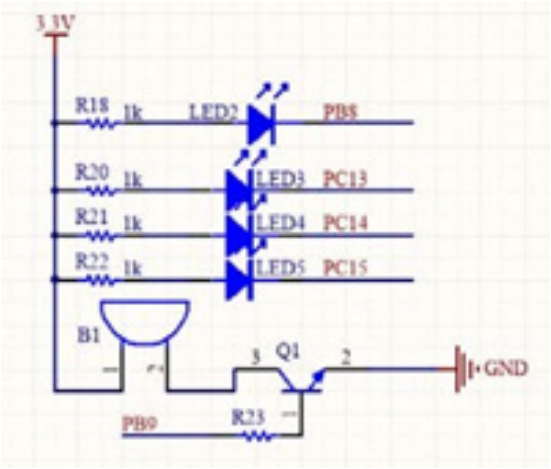

Figure 4. Buzzer and LED circuit.

2.2 THM3070 and its peripheral circuits

2.2.1 THM3070 circuit

THM3070 is a smart card read-write chip working at 13.56 MHz, with built-in power amplifier driver and adjustable transmission power. It conforms to ISO/IEC14443 TypeA/B and ISO/IEC 15693 standards, supports data transmission rates of 106 kbit/s, 21 2kbit/s, 424 kbit/s and 848 kbit/s, and has a maximum length of 256 bytes. The communication interface between the external controller and THM3070 has SPI mode or IDR mode, in which IDR interface can only be used for the second generation ID card security module. This system mainly uses SPI interface. The external controller communicates with THM3070 through SPI protocol to realize read-write memory sender, read-write data, send-receive control, baud rate control and protocol selection.

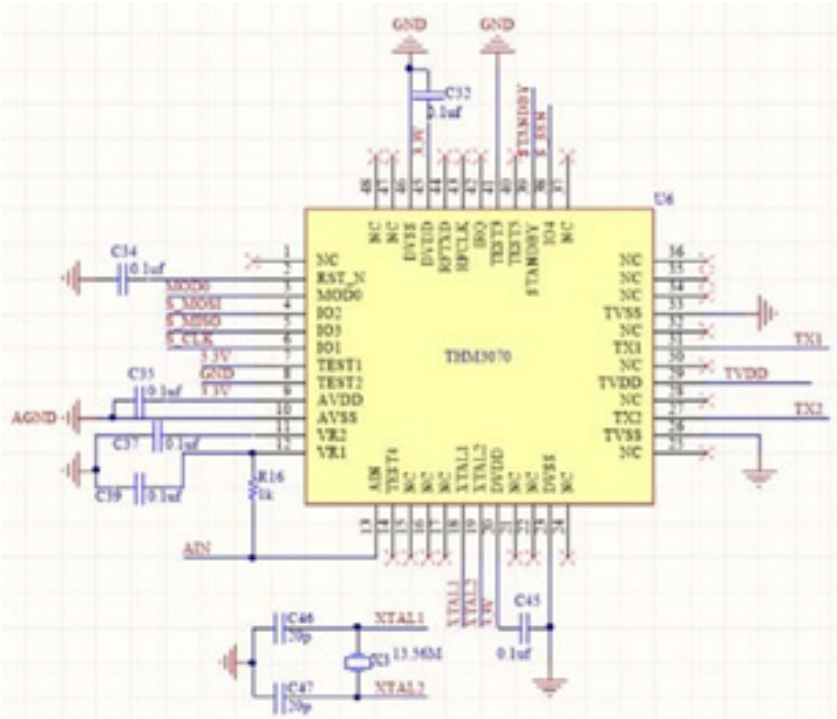

Figure 5. THM3070 circuit.

2.2.2 Filter and signal transmission circuit

As shown in Figure 6, TX1 and TX2 are respectively connected to the 31 and 27 pins of THM3070, which are the outputs of the chip power amplifier pins. The output signals are filtered by L1, L2, C15, C16, C21 and C22 and then contact with the pins of the smart card chip through the J14 interface.

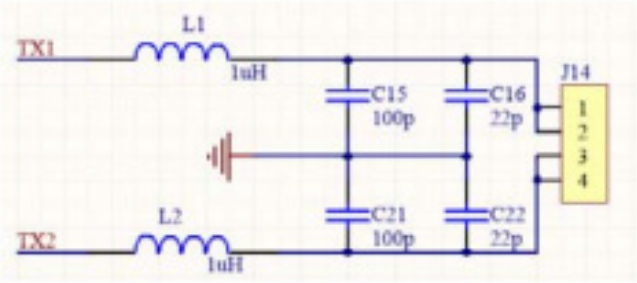

Figure 6. Filter and signal transmission circuit

3. Related program design of reader

In this design, the communication between the main controller and THM3070 is realized by SPI protocol. SPI (Serial Peripheral Interface-Serial Peripheral Interface) allows MCU to communicate and exchange data with various

peripheral devices in serial mode. SPI bus usually consists of 4 lines, namely serial clock line (SCK), master output and slave input line (MOSI), master input and slave output line (MISO) and slave select line (SSN)[3]. The THM3070 SPI interface supports clock normal low, rising edge valid timing, and SSN to remain low within one frame of data.

When writing register data, STM32 first issues the address to be written and then follows the data to be written. During the operation period. SSN must remain low, and THM3070 samples data on the rising edge of each clock. When reading register data, STM32 issues the address to be read by MOSI, MISO outputs the data in the corresponding address, THM3070 outputs the data on the falling edge of the clock, STM32 samples the data on the rising edge of each clock.

When writing buffer data, the write address is fixed at 0x80, and the data immediately following it cannot exceed 256 bytes. During operation, SSN needs to be kept low at all times. When reading buffer data, the read data address is fixed to 0x00 and SSN is kept low during operation.

4. Conclusion

This paper introduces in detail the hardware and software design of the reader-writer based on STM32 smart card chip. The main controller adopts STM32F103CBT6. The chip supports full speed USB communication rate of 12Mbps, which improves the data transmission rate of the host computer and reader-writer. The card reading chip adopts THM3070 of Uni-Light Co., Ltd. which supports 280 ISO/IEC144443 TypeA and TypeB standards and ISO/IEC15693 standards. In view of the disadvantages of low speed and poor interrupt response when traditional reader-writer uses serial port to communicate with host computer, this design adopts USB CCID protocol to re-package the communication data packets between host computer and reader-writer, and realizes data interaction between host computer application program and reader-writer conforming to PC/SC specification.

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