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An Analyses of Schottky Structure with Lead Monoxide Layer

Abstract: Al/ lead monoxide (PbO) /*p*-Si structures were consructed to research the electrical properties of PbO interlayer and the conductance-voltage (*G*-*V*) and capacitance-voltage (*C*-*V*) characteristics of these structures at room temperature have been studied at 600kHz, 800kHz and 1MHz. The study of barrier height $\phi_b(C-V)$, series resistance (R_s) and interface states density (D_{it}) using *G*-*V* and *C*-*V* graphs in these structures has been reported. *G* and *C* measurements were obtained to be dependent on frequency and bias voltage.

Keywords: Oxide layer, Schottky barrier diode, electrical properties, interface states

Introduction

PbO widely used in gas sensors, pigments, storage batteries and paints [1,2] is an important industrial material and has many crystalline forms such as Pb_3O_4, Pb_2O_3, PbO (α,β) and PbO_2 (α,β) [3]. The lead to oxygen ratio implies color of PbO and band gap of PbO. It has two phases: 1. Red α-PbO at low temperature is called as litharge and stable 2) Yellow β-PbO at high temperature is called as massicot and stable [4]. From α-PbO to β-PbO phase transition become about 763 K. In addition β-PbO at room temperature may appear even [5]. PbO which has high carrier mobilities, conductivities and strong absorption cross sections, and are useful photovoltaic materials [6–7].

Oxides films vary both dielectric and electrical properties of Barrier diodes (BD) when oxide films are inserted between metal and semiconductor. If bias voltage is applied across BD, this applied voltage was shared the depletion layer of BD, series resistance and combination of interfacial insulator.

The reliability and performance of these structures and the diode characteristics as $\phi_b(C-V)$, R_s, ideality factor and D_{it} were influenced because of the existence of interfacial insulator and these structures change into a Metal–Insulator–Semiconductor. The forward bias *I*–*V* graphs at large voltages diverge fairly from linearity because of effects of the electrical parameters while the forward bias *I*–*V* graphs at low voltages are linear in the semilogarithmic scale [8].

Electrical characteristics are analyzed using capacitance and conductance–frequency techniques. In order to discern the influences of trapping at interfacial insulator layer-semiconductor interface, a research of alternating current conductance of Metal-Insulator-Semiconductor capacitors found by Goetzberger and Nicollian can be used for conductance measurement. It was pointed that capacitance decreased with increasing frequencies. The intermediate and low frequency *G*–*V* and *C*–*V* measurements show these effects. Interface states inducing a bending of C^{-2} - *V* apart from increasing the ideality factor can also effect the *C*–*V* properties for MIS structures. An increase in capacitance with an increase in forward bias is seen from *C*–*V* graph [9].

The Hill-Coleman technique which is the most important among various measurement techniques has been developed for D_{it}. Some authors have used this technique which is a forceful tool for deducing D_{it} [10-13].

Generally, *G*–*V* and *C*–*V* graphs are frequency independent in the ideal case [13–23]. Because of presence of an interfacial layer, this ideal case is often disturbed. Accordingly, frequency dependent electrical properties are crucial to study reliable and accurate results. *C*–*V* characteristics of BD considering series resistance effect have been researched by Chattopadhyay and co-workers and an anomalous peak in the forward bias *C*–*V* graph is observed [23-25].

In this study, PbO was deposited on *p*-Si by evaporation technique so that Al/ PbO/ *p*-Si diodes were

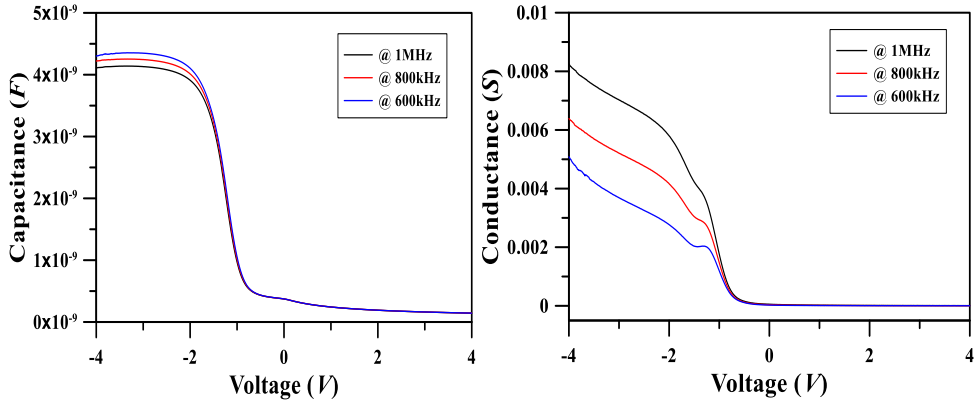
obtained to a high performance. The effects of R_s and D_{it} on G and C values were analyzed using G-V and C-V measurements of these structures at 600kHz, 800kHz and 1MHz.

Experimental

Experimental methods are explained in the Ref [8]. While It was shown using I-V measurements to investigate the effects of R_s, $\phi_b(C-V)$ and D_{it} on G and C values has been studied using C-V measurements in this study.

Results and Discussion

The voltage- dependence of the measured G–V and C–V at 600kHz, 800kHz and 1MHz for Al/ PbO /p-Si are shown in Fig.1 a and b. G–V and C–V curves have defined three regimes as inversion –depletion– accumulation regions as seen in Fig.1 a and b.



(a) (b)

Figure 1. **a**) Capacitance and **b**) Conductance characteristics vs voltage of Al/ PbO/ p-Si for 600kHz, 800kHz and 1MHz .

D_{it}, R_s and thickness and formation of oxide layer affect C and G values. D_{it} can be eliminated at $f \geq 500$kHz [25-29] because charges at interface states can not track an a.c. signal and D_{it} is in equilibrium with the semiconductor. $1/C^2$-V graphs giving a straight line in a wide range of applied bias voltages are shown at 600kHz, 800kHz and 1MHz in Fig.2a,b and c. The slope gives to the localized doping concentration [29]. This is came from the standard Schottky–Mott analysis [16] where doping concentration in a semiconductor can be obtained in the depletion region via

$$\frac{\partial(C^{-2})}{\partial V} = \frac{2}{A^2 \varepsilon_s \varepsilon_0 q N_A} \quad (1)$$

where A , C, ε_s , ε_0 , V and N_A are defined the area of device, the capacitance in the depletion region, semiconductor permittivity (ε_S = 11.8ε_0 for Si), the vacuum permittivity (ε_0 = 8.85×10^{-12} F/m), gate voltage and the ionized traps like-acceptor, respectiveley. [24].

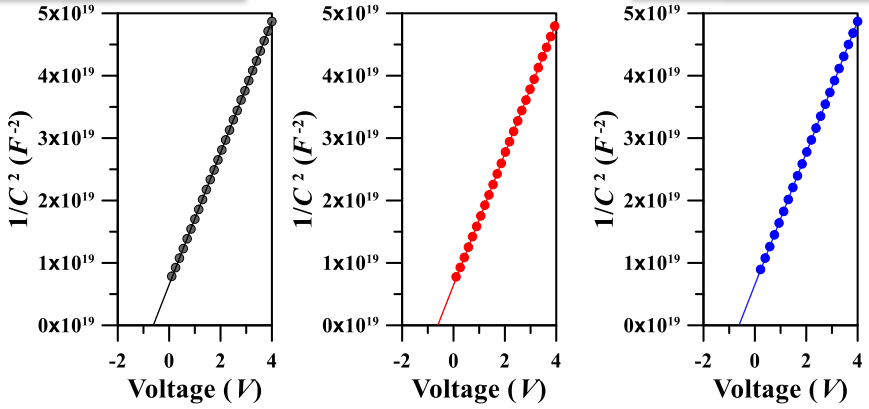


Figure 2. C^{-2}-V plots of Al/ PbO/ p-Si a) at 1MHz b) at 800kHz and c) at 600kHz.

The barrier height is described as.

$$\phi_b(C-V) = V_{bi} + E_F - \Delta\phi_b \quad (2)$$

The image force lowering is defined from [24].

$$\Delta\phi_b = \left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2} \quad (3)$$

where the maximum electric field is given by [13]:

$$E_m = \frac{2qV_{bi}N_A}{\varepsilon_s\varepsilon_0} \quad (4)$$

E_m values are found as 6.03 ×10^4 V/cm for 600 kHz and 800kHz, 6.06 ×10^4 V/cm for 1MHz. Energy difference between the bulk Fermi level (E_F) and valance band edge is defined as

$$E_F = \frac{TK}{q}\ln\left(\frac{N_A}{N_V}\right) \quad (5)$$

and

$$N_v = 4.82\times10^{15}T^{3/2}\left(\frac{m_h^*}{m_0}\right)^{3/2} \quad (6)$$

Where m_h^* ($m_h^* = 0.16m_0$), N_v and m_0 are defined as the effective mass of holes, the effective density states in valance band for p-Si and the rest mass of the electron, respectively [23].

Initially, V_{bi} obtained from the extrapolation of C^{-2}-V graph to the voltage axis is calculated 0.62 negative value for Al / PbO / p-Si structures. E_F, $\Delta\phi_b$ and N_A values were calculated as 0.158 eV, 0.027 eV and 1.84×10^{16} for 600kHz, 800kHz and 1 MHz, respectively. Using Eq. 2, $\phi_b(C-V)$ were found as 0.806 eV, 0.802 eV and 0.810 eV at 600kHz, 800kHz and 1MHz, respectively. $\phi_b(C-V)$ and $\phi_b(I-V)$ obtained values for the Al/ PbO/ p-Si structures are not the same because of different nature of I–V and C–V measurement techniques [8]. C is insensible to potential fluctuations on a length scale of less than the space charge region and C–V technique means over the whole area and measures to explain $\phi_b(C-V)$. The interface current (DC) depends on the detailed distribution and the barrier height at the interface [24-34]. The trap states in semiconductor and presence of the interfacial layer may cause the diffferenc between $\phi_b(C-V)$ values of these structure. As a result, the $\phi_b(I-V)$ values found by I–V characteristics [8] are smaller than the $\phi_b(C-V)$ values found by C^{-2}-V characteristics.

The depletion layer width (W_d) is given as

$$W_d = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_A}} \quad (7)$$

W_d values were found 2.137 10^{-5} cm, 2.135 10^{-5} cm and 2.151 10^{-5} cm for 600kHz, 800kHz and 1MHz, respectively.

Nicollian and Brews [15,17] were described admittance method providing the indicating of R_s in the whole measured range diode for determining voltage dependence of R_s values. According to this method, R_s values at $f \geq 500$ kHz correspond to series resistance values in strong accumulation region for MOS or MIS structures and these values can be obtained from the measured G_m and C_m values. It is defined as

$$R_s = \frac{G_m}{G_m^{\,2} + \omega^2 C_m^{\,2}} \quad (8)$$

Where ω , G_m and C_m are defined as the angular frequency, the measured G and C in the accumulation region.

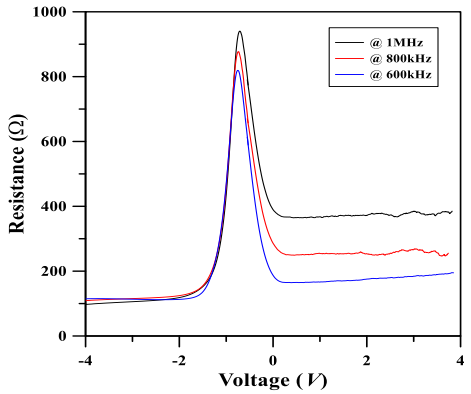


Figure 3. The voltage - dependence of R_s at 600kHz, 800kHz and 1MHz.

The voltage dependent R_s values from about -4 V to -4 V are found at high frequencies and give a distinguishable peak as seen in Fig.3.

In this study, D_{it} values using the Hille-Coleman method are calculated to understand the electrical properties of the interface [15]. With regard to this method, D_{it} is given as

$$D_{it} = \frac{2}{qA}\left(\frac{(G_{c,\max}/\omega)}{(G_{c,\max}/\omega C_i)^2 + (1 - C_c/C_i)^2}\right) \quad (9)$$

where $G_{c,max}$, C_c and C_i are defined as the maximum in the corrected G-V curve; the capacitance of the diodes corresponding to $G_{c,max}$ and the capacitance of interfacial layer [29]. C_i value using the G - V and C-V measurements in accumulation region for 1 MHz is found as [15]

$$C_i = C_m\left[1 + \frac{G_m^{\,2}}{(\omega C_m)^2}\right] = \frac{\varepsilon_i \varepsilon_0 A}{d} \quad (10)$$

C_i and D_{it} values are calculated 4.24 nF, 2.36 x10^{14} 1 / eV cm^2 at 600 kHz, 1.41x10^{14} at 800 kHz and 9.82 x10^{13} 1 / eV cm^2 at 1 MHz for Al/ PbO/ p-Si structures, respectively. However, D_{it} (10^{13}–10^{14} 1 / eV cm^2) calculated values are not high enough to pin the Fermi level of the Si substrate disrupting the device operation [21–29]. As a result, the construction of an MIS device can not be prevented the interface traps and defects

The interface defects and traps can not prevent the construction of MIS. D_{it} values changed from 4.17×10^{11} to 5.29×10^{14} 1 / eV cm^2 for oxides and polymers layers were found S.Bilge Ocak et. al. [20,21,25,29]. D_{it} properties for Sn/methylred/p-Si/Al structures have been investigated and these values have been changed from 1.68×10^{12} to 1.80×10^{12} 1 / eV cm^2 by Aydin and Turut [35].

It is shown that the oxide layer inserted into semiconductor and metal change interface properties of Al / p-Si structures and cause an important modification of D_{it} values even if they appear in non-reactive and sudden [35]. PbO oxide layer effects $\phi_b(C-V)$ values fairly upon the modification of the semiconductor surfaces and D_{it} will be occured by chemical interaction at the interface of PbO oxide layer to p-Si and oxide interface states.

Conclusions

Al/ PbO/ p-Si structures were formed and researched the electrical characteristics at room temperature. C–V and G–V characteristics of these structures were studied for 600kHz, 800kHz and 1MHz. It is shown that the forward and reverse bias G–V and C–V values were sensitive to voltage and frequency. A behaviour of G and C is ascribed to particular distribution of D_{it} at series resistance and the oxide. It is seen that R_s varies from region to region, obtains from the G-V and C-V measurements in strong accumulation regions at high frequency and is dependent on voltage and frequency. It is considered that trap charges have enough energy to run away the traps at the metal-semiconductor interface in the Si band gap and D_{it} can not track ac signal.

Experimental results imply that D_{it} location between R_s and Si/PbO has an important on electrical properties of Al/ PbO/ p-Si. The fabricated these structures can be utilise as a good electronic material combination for possible applications. It is suggested that PbO interlayer for the novel MOS devices might be

taken into consideration among other oxides, as a potential thin film.

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